

Remarks/Arguments

With reference to the Office Action of October 3, 2005, Applicants offer the following remarks.

Art Rejections

In the Office Action of October 3, the following art rejections were made:

Claim Number	§102 – USP 6,084,849 to Durig	§103 --- Durig in view of Shum	§103 --- Durig in view of Batcher
1	X		
2	X		
3		X	
4		X	
5		X	
6	X		
7			X
8	X		
9	X		
10	X		
11	X		
12	X		

The Art of Record

1. United States Patent 6,084,849 to Durig et al. Shape Memory Alloy Recording Medium, Storage Devices Based Thereon, And Method For Using These Storage Devices describes a storage medium for scanning probe storage devices. Durig's storage medium comprises a substrate carrying a shape memory alloy layer. The shape memory alloy layer is chosen such that an indent can be formed by mechanically deforming said shape memory alloy layer, when a local probe of said scanning probe system exerts pressure on said alloy layer. An indent can be removed by locally heating the shape memory alloy layer to its

transformation temperature (Tc) or above such that the shape memory alloy returns to its Martensite form.

The following excerpts of Durig et al have been cited in the Office Action:

1) Column 1, lines 21-33:

There is a demand for storage devices having storage capacity of more than 1 Terabit. Further criteria for such storage devices are: power consumption, overall weight and size, reliability, data security, and shock resistance (if used in portable computer systems).

With a storage device which combines the capacity of a rotating memory with the speed, size, power consumption and reliability of solid state memories, computers would take another quantum leap in performance and compactness.

The development of scanning tunneling and atomic force microscopes has led to first storage systems which make use of local probes.

2) Column 1, lines 41-49:

In U.S. Pat. No. 5,307,311 a memory device is described which makes use of a very large set of independently operating subdevices. It employs an array of hundreds of microcantilevers having an area in which bits are stored. Opposite to these cantilevers there are hundreds of read/write heads which are similar in nature to scanning tunneling or atomic force microscope scanning tips. Each cantilever is moved in an oscillatory manner such that the respective read/write head scans over the bits stored thereon

3) Column 1, lines 65-67:

Current pulses induced by voltage pulses sufficient to selectively heat discrete areas of the state-transformable material are applied to a STM tip.

4) Column 6, lines 4-12:

A scanning probe storage system in accordance with the present invention, further comprises local probe array with cantilevers 52.1-52.4, as illustrated in FIG. 7. Each cantilever carries at least one tip for interaction with the storage fields 54.1-54.4 of the storage medium. The array of cantilevers with the respective tips is scanned as a whole over the corresponding storage fields 54.1-54.4 and the data in each storage field are addressed quasi-simultaneously.

2. United States Patent 6,865,645 to Shum et al. for Program Store Compare Handling Between Instruction And Operand Caches describes a method of supporting programs that include instructions that

modify subsequent instructions in a multi-processor system having a central processing unit including an execution unit, and instruction unit and a plurality of caches including a separate instruction and operand cache.

The following passages in Shum have been cited in the Office Action:

1) Column 1, lines 48-61:

In a multiprocessor computer system, it is important to provide a coherent memory system, that is, to cause writes to each individual memory location to be serialized in some order for all central processing units. For example, assume a location in memory is modified by a sequence of write operations to take on the values: 1, 2, 3, 4. In a cache-coherent system, all central processing units will observe the writing to a given location to take place in the order shown. However, it is possible for a central processing unit to miss observing a write to the memory location. A given central processing unit reading the memory location could see the sequence 1, 3, 4, missing the update to the value 2. A multiprocessor system that implements these properties is said to be "coherent."

2) Column 2, lines 4 – 14:

The cache coherency protocol allows shared access by the instruction cache and the operand cache to a cache block if it has read only status. In addition, the cache coherency protocol allows access by the operand cache and prevents access by the instruction cache to a cache block if it has exclusive status.

3) Column 2, lines 26-28:

The FIGURE depicts a multi-processor system 10 including separate instruction cache (I-cache) 50 and Data or Operand cache (D-cache) 40.

4) Column 2, lines 43-53:

As a consequence, whenever a particular central processing unit 100 attempts to write to a memory location, it must first inform all other central processing units 100 of its desire to write to the location and receive permission from all other processing elements to carry out the write. On the other hand, if a particular central processing unit 100 attempts to read from a memory location, it must inform at least the central processing unit 100 currently having write permission to the subject memory location, and receive permission to carry out the read.

3. United States Patent 4,314,349 to Batcher for Processing Element For Parallel Array Processors describes a processing element that is the basic building block of a massively-parallel processor. As described

by Batcher, the processing element includes an arithmetic sub-unit comprising registers for operands, a sum-bit register, a carry-bit register, a shift register of selectively variable length, and a full adder. A logic network is included with each processing element for performing the basic Boolean logic functions between two bits of data. There is also included a multiplexer for intercommunicating with neighboring processing elements and a register for receiving data from and transferring data to neighboring processing elements. Each such processing element includes its own random access memory which communicates with the arithmetic sub-unit and the logic network of the processing element.

The only segment of Batcher cited in the Office Action is Column 1, line 66 to column 2, line 3:

Further, it is desirable that the massive array of processing elements be capable of intercommunication such that data may be moved between and among at least neighboring processing elements. Further, it is desirable that each processing element be capable of performing all of the Boolean operations possible between two bits of data, and that each such processing element include its own random access memory

4. United States Patent 5,307,311 to Sliwa, for Microvibratory Memory Device describes a memory device whose media scanning is vibrationally (cyclic harmonic vibration) or inertially (one-time pulsed read/write) driven is provided. The read-write device comprises a plurality of cantilevers, attached at one end and capable of vibrating. On the opposite end of each cantilever is disposed an array of storage bits. Opposite the surface of each cantilever having such a bit array is a read/write head which is similar in nature to a scanning tunneling microscopy or atomic force microscopy scanning-tip. Electronic support circuitry is provided to implement the memory device of the invention. Such circuitry includes a microprocessor, a multiplexer/demultiplexer, a group of circuits comprising power supplies, sensing circuits and digital/analog and analog/digital conversion

circuits, and switching means to permit all of the previous functions to be properly addressed to/from the correct bit/array(s) and mating subdevice(s).

The cited segments of Sliwa include:

1) Column 1, lines 67-68:

Each cantilever has disposed on its surface an array of storage bits called a bit array

2). Column 2, lines 6-17:

Each bit-array is translated relative to its adjacent read/write head in a sweeping motion caused by the oscillatory vibration of its respective cantilever.

3). Column 2, lines 22-25:

Choices exist for placing either the bit-array(s) or the read/write head on the moving cantilever with its counterpart being disposed on the remaining opposite surface.

4). Column 2, lines 58-62:

If the areal arrays are to be physically addressed, one requires relative areal scanning motion of the bit array relative to the read/write head which is dedicated to that bit array.

5). Column 4, lines 34-68:

Cantilevers can be set in resonant motion and that motion can be maintained with minimal ongoing excitation pulses.

When using an oscillating plate to support many bit arrays, one is presented with certain tradeoffs which can be avoided in the cantilever approach. Firstly, for a swinging plate to be internally rigid, it must have substantial depth so as not to introduce unwanted plate-mode vibrations which would complicate Z-axis separation control. This substantial depth results in substantial mass which must be moved at high frequency through substantial displacements. This can result in more power being consumed than in the cantilever approach for the same memory implementation. One may consider a hollowing of the plate to reduce its mass to help in this situation. The internal flexing of swinging plates can be totally avoided by not swinging or sliding the plate but by having the rigidly attached plate distort in shearing motion. A plate not in swinging motion but in shearing motion is far stiffer than a cantilever in bending motion. A plate in shear motion across its thickness of thickness equal to the cantilever height has far higher resonant frequency than the cantilever. The result is small scan distances at high frequency.

In order to obtain large cantilever-size motions with plates, it is best to suspend the plate on its edges with springs which cause the plate to oscillate in its own plane. This is drastically different than gripping a plate by its back surface and causing it to vibrate in shear. In the latter case, large oscillations require a very thick plate, whereas in the former

case, wherein the plate simply swings but does not distort in shear, large amplitudes can easily be had by using "soft" low-stiffness micromachined springs of great depth, thus of large Z-axis rigidity.

6). Column 11, lines 16-24:

One may choose to utilize one or more cantilever devices to read a spatial reference pattern of positional data written on its bit-array, thus providing a signal which is a function of unwanted displacement and acceleration to the corrective means which may, as described, consist of corrective damping or cancellation resonator motions. The same reference pattern may aid in tip position determination on all cantilevers, as is done with tracks and sectors on magnetic disk drives.

Applicants' Claimed Invention

Status of the Claims.

Claims 1-12 were originally presented for examination. All twelve claims were rejected in the Office Action of October 3, 2005.

Applicants have amended independent claims 1 and 10, and cancelled claims 2, 3, 9, 11, and 12. This is a reduction of five claims, from twelve claims to seven claims.

Exemplary Claim

Claim 1, as amended, is exemplary.

1. (Currently Amended) A data processing system comprising: a CPU, a storage surface, a local probe storage array having a plurality of sensors for reading data from [[[a]]] the storage surface; a plurality of data processing elements mounted on the storage array and each connected to different sensor of the array for processing data read by said connected sensor, said storage surface comprising a plurality of data fields each data field corresponding to a different one of the sensors, each data field having a matrix of bit storage locations

individually addressable by a corresponding sensor, and the storage surface comprising a user data portion dedicated to storage of user data for manipulation by the processing elements, and a program code portion dedicated to storage of program code for configuring the processing elements to manipulate the user data, said CPU mounted on said array and switchable between different functions, with each sensor connected to a corresponding point on the CPU via a direct local electrical connection, and a random access memory mounted on and connected to the CPU.

where the elements of the claim are:

A data processing system comprising:

a CPU,

a storage surface;

a local probe storage array having a plurality of sensors for reading data from the storage surface;

a plurality of data processing elements mounted on the storage array and each connected to different sensor of the array for processing data read by said connected sensor,

said storage surface comprising a plurality of data fields each data field corresponding to a different one of the sensors,

each data field having a matrix of bit storage locations individually addressable by a corresponding sensor,

and the storage surface comprising

a user data portion dedicated to storage of user data for manipulation by the processing elements, and

a program code portion dedicated to storage of program code for configuring the processing elements to manipulate the user data,

said CPU mounted on said array and switchable between different functions,

with each sensor connected to a corresponding point on the CPU via a direct local electrical connection, and

a random access memory mounted on and connected to the CPU.

Discussion: Art Rejection

The overarching issue is whether the claims, as limited by the newly added clauses and limitations are allowable over the art of record.

Durig (Column 6, lines 4-12) describes

A scanning probe storage system in accordance with the present invention, further comprises local probe array with cantilevers 52.1-52.4, as illustrated in FIG. 7. Each cantilever carries at least one tip for interaction with the storage fields 54.1-54.4 of the storage medium. The array of cantilevers with the respective tips is scanned as a whole over the corresponding storage fields 54.1-54.4 and the data in each storage field are addressed quasi-simultaneously.

Batcher, column 1, line 66, to column 2, line 3, describes

Further, it is desirable that the massive array of processing elements be capable of intercommunication such that data may be moved between and among at least neighboring processing elements. Further, it is desirable that each processing element be capable of performing all of

the Boolean operations possible between two bits of data, and that each such processing element include its own random access memory

Sliwa, column 4, lines 34-68 describes:

Cantilevers can be set in resonant motion and that motion can be maintained with minimal ongoing excitation pulses.

When using an oscillating plate to support many bit arrays, one is presented with certain tradeoffs which can be avoided in the cantilever approach. Firstly, for a swinging plate to be internally rigid, it must have substantial depth so as not to introduce unwanted plate-mode vibrations which would complicate Z-axis separation control. This substantial depth results in substantial mass which must be moved at high frequency through substantial displacements. This can result in more power being consumed than in the cantilever approach for the same memory implementation. One may consider a hollowing of the plate to reduce its mass to help in this situation. The internal flexing of swinging plates can be totally avoided by not swinging or sliding the plate but by having the rigidly attached plate distort in shearing motion. A plate not in swinging motion but in shearing motion is far stiffer than a cantilever in bending motion. A plate in shear motion across its thickness of thickness equal to the cantilever height has far higher resonant frequency than the cantilever. The result is small scan distances at high frequency.

In order to obtain large cantilever-size motions with plates, it is best to suspend the plate on its edges with springs which cause the plate to oscillate in its own plane. This is drastically different than gripping a plate by its back surface and causing it to vibrate in shear. In the latter case, large oscillations require a very thick plate, whereas in the former case, wherein the plate simply swings but does not distort in shear, large amplitudes can easily be had by using "soft" low-stiffness micromachined springs of great depth, thus of large Z-axis rigidity.

And Sliwa's column 11, lines 16-24 describes

One may choose to utilize one or more cantilever devices to read a spatial reference pattern of positional data written on its bit-array, thus providing a signal which is a function of unwanted displacement and acceleration to the corrective means which may, as described, consist of corrective damping or cancellation resonator motions. The same reference pattern may aid in tip position determination on all cantilevers, as is done with tracks and sectors on magnetic disk drives.

But, these citations, even with the other citations neither teach nor suggest applicants' claimed combination of sensors and surface and their interaction through the geometry of the storage surface and the claimed features of the sensors.

The invention resides in the interaction of a combination of elements. The scope of the invention is defined by the metes and bounds of the explicit language of the claims. Neither Durig nor Shum nor Batchner nor Sliwa, either alone, or in combination with each other, teach or suggest the claimed invention. The combination of these eleven elements in amended claim 1 is neither taught nor suggested by the art of record. Thus, the claims are properly allowable to the Applicants.

More than just the mere presence or absence of all of the elements, or any sub set of them, the references fail to teach the effect of the combination

Conclusion

Based on the above discussion, it is respectfully submitted that the pending claims describe an invention that is statutory subject matter and is properly allowable to the Applicants.

If any issues remain unresolved despite the present amendment, the Examiner is requested to telephone Applicants' Attorney at the telephone number shown below to arrange for a telephonic interview before issuing another Office Action.

Applicants would like to take this opportunity to thank the Examiner for a thorough and competent examination and for courtesies extended to Applicants' Attorney.

Respectfully Submitted


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